QUERY CONTR	OL FORM	RTIS U	SE ONLY		
Application No.	10/066 182	Prepared by	Tabbins	Tracking Number	05895837
Examiner-GAU	Phan-2818	Date	3-30-04	Week Date	1-26-04
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JACKET											
a. Serial No.	1. Foreign Priority	k. Print Claim(s)	p. PTO-1449								
b. Applicant(s)	g. Disclaimer	I. Print Fig.	q. PTOL-85b								
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract								
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs								
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other								

SPECIFICATION	MESSAGE Patent claim 30 Coriginal claim
a. Page Missing	41) depends on canceled original chimk;
b. Text Continuity	
c. Holes through Data	Patent claims 32-36 (original claims
d. Other Missing Text	43-47) depend on patent claim 39
e. Illegible Text	Coriginal claim 37), See claims
f. Duplicate Text	in amendment indexed in IFW dated
g. Brief Description	11-25-2083.
h. Sequence Listing	
i. Appendix	
j. Amendments	
k. Other	
CLAIMS	
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b. Improper Dependency	
c. Duplicate Numbers	Thank Tou
d. Incorrect Numbering	initials
e. Index Disagrees	RESPONSE DONE
f. Punctuation	
g. Amendments	
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i. Missing Text	·
j. Duplicate Text	
k. Other	
	initials 7P

Index of Claims

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Examiner

TRONG PHAN

Applicant(s)

MCCLURE, DAVID C.

Art Unit

2818

√	Rejected	-	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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means for placing on an external pad of the apparatus during a test mode of operation a current level corresponding to a voltage level appearing across the ferroelectric capacitor, said means comprising a first transistor having a control terminal coupled to a plate of the ferroelectric capacitor, a first conduction terminal coupled to the external pad and a second conduction terminal connected to a voltage reference, and a second transistor having a first conduction terminal connected to the external pad a voltage reference and a second conduction terminal connected to the first second conduction terminal of the first transistor, and a means for selectively activating the second transistor during the test mode of operation.

- 38. (Canceled).
- 39. (Canceled).
- 40. (Previously Added) The random access memory device of claim 1, wherein the current level placed on the external pad by the test circuitry is proportional to the voltage level appearing on the at least one bit line.
- 41. (Previously Added) The method of claim 16, wherein the current level provided to the pad is proportional to the voltage level appearing on the selected bit line.
- 42. (Previously Added) The apparatus of claim 22, wherein the current level placed on the external pad is proportional to the voltage level appearing on the at least one bit line.